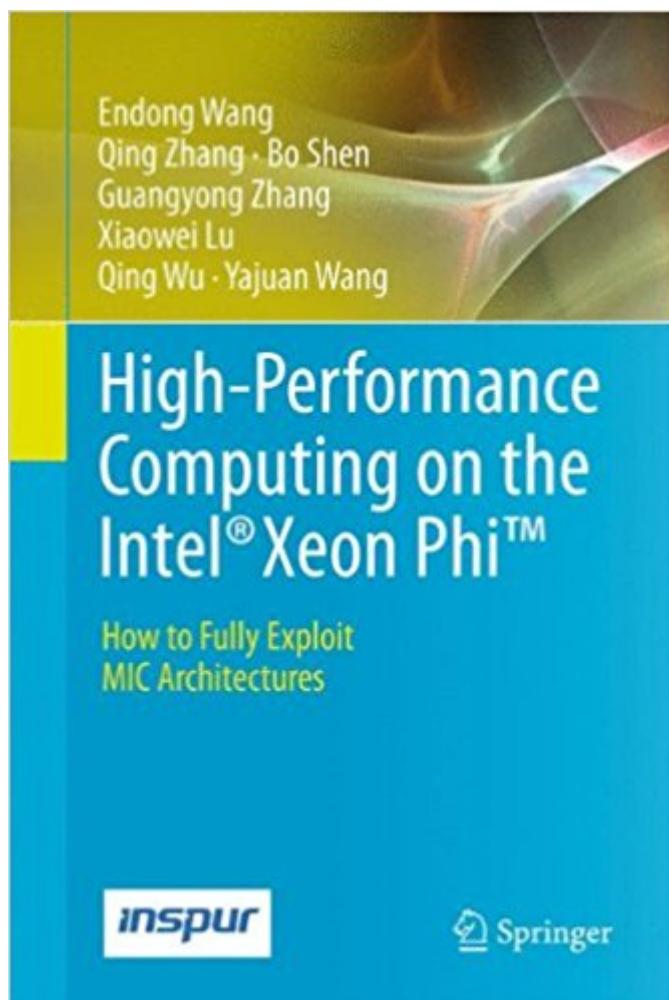


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# High-Performance Computing On The Intel® Xeon Phi™: How To Fully Exploit MIC Architectures



## Synopsis

The aim of this book is to explain to high-performance computing (HPC) developers how to utilize the Intel® Xeon Phi™ series products efficiently. To that end, it introduces some computing grammar, programming technology and optimization methods for using many-integrated-core (MIC) platforms and also offers tips and tricks for actual use, based on the authors' first-hand optimization experience. The material is organized in three sections. The first section, "Basics of MIC", introduces the fundamentals of MIC architecture and programming, including the specific Intel MIC programming environment. Next, the section on "Performance Optimization" explains general MIC optimization techniques, which are then illustrated step-by-step using the classical parallel programming example of matrix multiplication. Finally, "Project development" presents a set of practical and experience-driven methods for using parallel computing in application projects, including how to determine if a serial or parallel CPU program is suitable for MIC and how to transplant a program onto MIC. This book appeals to two main audiences: First, software developers for HPC applications as it will enable them to fully exploit the MIC architecture and thus achieve the extreme performance usually required in biological genetics, medical imaging, aerospace, meteorology and other areas of HPC. Second, students and researchers engaged in parallel and high-performance computing as it will guide them on how to push the limits of system performance for HPC applications.

## Book Information

Hardcover: 338 pages

Publisher: Springer; 2014 edition (June 26, 2014)

Language: English

ISBN-10: 3319064851

ISBN-13: 978-3319064857

Product Dimensions: 6.1 x 0.8 x 9.2 inches

Shipping Weight: 1.5 pounds (View shipping rates and policies)

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Endong Wang is the Director of the State Key Laboratory of High-Efficiency Server and Storage Technology at the Inspur-Intel China Parallel Computing Joint Lab and Senior Vice President of the Inspur Group Co., Ltd. Qing Zhang is the lead engineer of the Inspur-Intel China Parallel Computing Joint Lab and with his team he was among the first to work with the development environment of the Intel® Xeon processor and Intel® Xeon Phi™ coprocessor. Together they have several years of experience in HPC programming.

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